

## **Design of new power generating circuit for passive UHF RFID tag**

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### **ABSTRACT**

In this paper, we propose a new power generating circuit for passive ultra high frequency (UHF) RFID tag. The proposed power generating circuit consists of a RF limiter, a high power efficiency and high sensitivity full wave radio frequency (RF) wave rectifier and a low-power regulator with NMOS diodes work like a DC-limiter. The design method proposed in this study use one low drop out (LDO) regulator to provide tow output stable supply voltages vdd1 of value 1V for the digital section supply, and vdd2 of value 0.5V for the analog front-end section power supply. The proposed power generating circuit is optimized in terms of power consumption of RFID tag system to have a high operating range under conditions of 50 Ohm antenna, -24 dBm input RF power, 900MHz and 1 M DC, with low power dissipation and 29.15% large power conversion efficiency. The power generating circuit was designed, simulated and layouted in Cadence using TSMC 180 nm technology. The final design occupies approximately 0.25mm<sup>2</sup>.

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## **1. INTRODUCTION**

RFID (radio frequency identification) it is a technology uses electromagnetic waves to transmit the ID of objects. It is a technology operates in non line of sight environments. RFID technology is becoming a part of our every life, at work in supermarkets at home and it can be implanted in animal or human bodies [1]. An RFID system consists of three main elements, an RFID tag/transponder, a reader or a transceiver contains an antenna and an electronic circuit that emits an electromagnetic wave (power) to active the passive RFID tag and a host system. In general, there are three types of RFID tags, an active tag, a semi active tag (semi passive tag) and a passive tag which powered from the received RF signal [2]. One of the most parameters to determine the communication range of the RFID system is the frequency. In the ultra-high frequency range frequencies can vary from 433 MHz to 2.45 GHz. frequency depends on location; for example, 868 MHz is only used in Europe, when 900 to 928 MHz is used in Canada and the USA.

The ultra high frequency (UHF) passive RFID tags have many advantages like their low cost, their low power consumption, their longer distance of operation, small antenna size and high data rate [3].

The principle of working of passive transponder is as follows, the demodulator extracts the amplitude shift keying (ASK) signal and demodulated form the baseband processor. The voltage rectifier circuit converts the received radio frequency (RF) signal from the antenna into a sufficiently DC voltage V<sub>r</sub>, this later is regulated by a voltage regulator circuit to generate a stable voltage supply to other sub-blocks of

the tag. The baseband processor manipulates the received binary data and then generates outputs according to the operations of the tag. Modulation technique is done (using ASK modulation) by varying the effective impedance of the antenna to backscatter signals back to the transceiver. The block diagram of a UHF RFID transponder is shown in Figure 1, it consists of an antenna, a digital part, and an analog front-end part contains, a modulator, a demodulator and an oscillator.

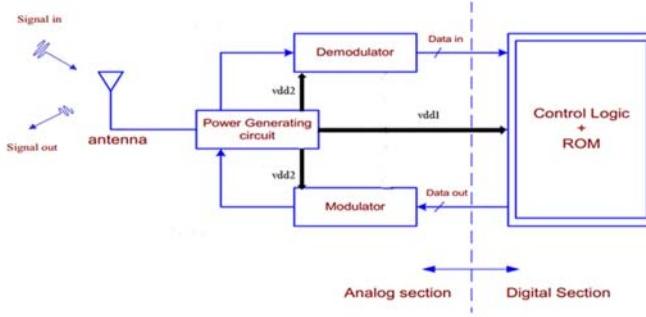


Figure 1. Passive RFID tag block diagram

For each analog front-end passive RFID tag we have a power generating circuit that can generate the power to each RFID tag sub-blocks. The efficiency of power generating circuit and communication range  $d$  of the RFID system depend on the voltage rectifier used in the voltage generator circuit. The Friis transmission (1) gives us the theoretical communication range  $d$  [4].

$$d = \frac{FREE_{space}}{4\pi} \sqrt{\frac{EIRP_{reader} \times G_{tag} \times PCE_{rectifier}}{P_{tag}}} \quad (1)$$

Where  $FREE_{space}$ ,  $EIRP_{reader}$ ,  $G_{tag}$ ,  $P_{tag}$  and  $PCE_{rectifier}$  are the free space wavelength, the effective isotropic radiated power of a reader, the gain of the tag antenna, the practicable operating power of an RFID tag is the power conversion efficiency of the rectifier used in the power generation circuit respectively.

The main challenges in RFID technology are: the minimizing of the power consumption of RFID tag, the increasing of the communication distance and the efficiency of voltage regulation. Many works were interested by the designing of the power generating circuit. Voltage rectifier with high power efficiency augments both the efficiency of the voltage regulation circuit and communication range  $d$  of RFID system. A voltage rectifier using Schottky diodes and capacitors has many advantages like their low junction capacitance, their small series resistance. Because of its less expensive and more compatible with standard CMOS technologies native NMOS transistor used in works [5], [6] and [7] is used instead Schottky diodes used in [8]. Both schottky diodes and native NMOS transistor rectifiers have many disadvantages; one of the common disadvantages of such rectifiers is the drop voltage of the output because of MOS transistors threshold voltage. The threshold voltage, not only reduces the power efficiency, but also decreases the output rectified voltage.

So to minimize the power consumption of the transponder and to increase the communication distance of RFID system, we propose a new approach which the RFID tag consumes a low power compared with other recent researches and with longer communication distance. In this approach we propose a low power voltage regulation circuit with two supply voltages from one low drop out (LDO) regulator using a new full wave RF rectifier which have advantages compared with schotky diodes and native NMOS transistor rectifiers, with the aim of eliminating the effect of threshold voltage of the pass transistor. The cross-coupled structure in voltage rectifier is considered for NMOS pass transistors and the capacitor and the transistor is used as the bootstrap circuit for neutralizing the effect of the PMOS pass transistors threshold voltage, which leads to reducing the chip area. In order to minimize the power consumption, we propose the reducing of the supply voltage of the analog section of a 0.5V while maintaining a supply voltage 1V to the digital core, using a new full wave RF rectifier with a high power efficiency and high sensitivity will increase the communication distance. The analog front-end section shown in Figure 1 which consists of proposed

power generation circuit which generates two output voltages using one LDO regulator with multiple output vdd1 and vdd2 their values are stable. vdd2 gets the power supply to the analog sub-blocks (modulator, demodulator, clock generator, ring oscillator), its value 0.5V. vdd1 generates a supply voltage to the digital sub-blocks (control logic and ROM), its value is 1V.

The proposed generating circuit proposed in this paper was designed in 180 nm CMOS process which consists of an RF voltage limiter circuit (protector) this later can protect the transponder system from damages caused to CMOS gate-oxide breakdown due to an excessive coupling voltage from the reader for a short operating distance. A high power efficiency and high sensitivity full wave RF wave rectifier is used to convert the RF received power to DC signals; the full wave rectifier is fully integrable and takes advantage of both passive and active multiplications to reduce the required input power. The minimum required input power is -24 dBm to generate supply voltage from a 50-Ohm antenna at 900 MHz, and a voltage regulator which regulates the output voltage of the rectifier to a preferred value.

## 2. POWER GENERATING CIRCUIT

The proposed power generating circuit consists of an RF voltage limiter, a high power efficiency and high sensitivity full wave rectifier and a voltage regulator. Theoretical analyzes and simulations of the circuits used to optimize the design are presented. The circuit shows the ability to generate stable DC voltages independent of the input power levels and it can be powered the passive UHF RFID tag. In this section, each sub-block of voltage regulation circuit is presented with more details.

### 2.1. Voltage RF limiter

The voltage at the input of the voltage rectifier can go from 350 mV to 20 V, depending on the proximity of the tag. To prevent the transistors of the inner circuit from being damaged at high voltage levels an RF limiter is used. The RF signal is detected by the RF\_in of the RF voltage limiter which is a stacked voltage diode referenced to the ground of the RFID tag. The output of RF limiter is given by (2):

$$RF_{out} = 2 \times V_{gs} + I_d \times R_2 \quad (2)$$

Where

$$V_{gs} = |V_{thp}| + \sqrt{\frac{2 \times I_d}{K'p \times \frac{W}{L}}} \quad (3)$$

With  $K'p$  and  $V_{thp}$  are transconductance parameter and the threshold voltage of PMOS transistor respectively. In (2) the value in the square root is minimized by using large transistor aspect ratios of transistors, with the  $I_d$  we can write:

$$RF_{out} = 2 \times |V_{thp}| \quad (4)$$

This means that when the RF signal exceeds  $2 \times |V_{thp}|$ , the RF voltage will reduce the actual voltage, above  $2 \times |V_{thp}|$ , the additional voltage appearing at the gate of NMOS transistor N1. After a certain limit of the transistor, N1 gradually turns on. Once N1 is fully activated, PMOS transistor P3 starts to decrease. To prevent the RF signal from being completely limited, a resistor R3 is used to maintain a voltage drop on the RF signal and N1 drain. When the gate voltage of P3 continues to drop as a result of switching N1, P3 starts to turn on. At this time, transistor P3 acts as a shunt and limits the increase of any applied RF signal. Figure 3 shows the amplitude of input signal after using proposed voltage limiter.

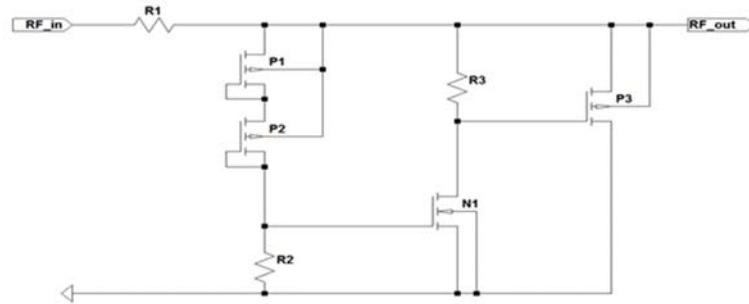
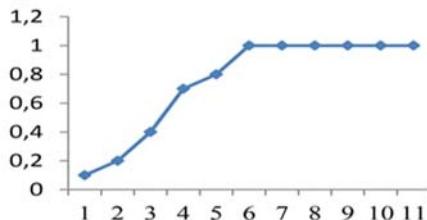


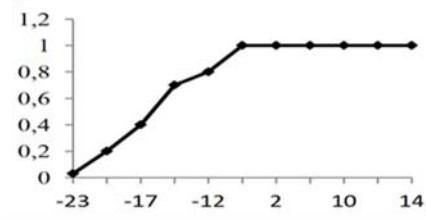
Figure 2. RF voltage limiter circuit

Voltage after RF limiter



(a)

Voltage after RF limiter



(b)

Figure 3. (a) Input voltage before RF limiter, (b) Input power before RF limiter (dBm)

## 2.2. Full wave RF rectifier

The voltage rectifier is a circuit converts the RF incident signal to a DC signal with very small ripples. It comes after the RF voltage limiter.

To improve power efficiency, the proposed full wave RF rectifier shown in Figure 6 uses the combination of the bootstrap circuit (capacitor  $C_B$  and transistor  $M_7$ ) with the cross-coupled structure [9]. Transistors  $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4$  are replaced by the transistors connected on diode of the conventional bridge rectifier and conduct the current path from the input source to the output load. Transistors  $M_1$  and  $M_2$  with the cross-coupled structure have the channel resistivity lower than their activation time. To improve the efficiency and the output voltage, the bootstrap is used to cancel the threshold voltage of the PMOS transistors. The bootstrap circuit is built using the capacitor  $C_B$  with transistor  $M_7$ . In this proposed topology, the gates of the transistors  $M_3$  and  $M_4$  and  $M_7$  are connected to each other (transistors connected on diode), the gates of transistors are connected with the output of the voltage rectifier to reduce the effect of the threshold voltage of  $M_3$  and  $M_4$ , PMOS pass transistors. The current of the input source charges boths the output capacitor and the capacitor  $C_B$  by  $M_5$  and  $M_6$ . The voltage accros the capacitor  $C_B$  can be suitable for the complete conductivity of the PMOS pass transistors. To reduce the leakage current, the sizes of the positive half-cycle, when the input voltage ( $V_{RF+}$ ) is larger than the output voltage, the current loads the output capacitor by  $M_5$ , the transistor connected to the diode. The voltage of the output capacitor and the capacitor  $C_B$  is given as follows: (6) and (15).

$$V_{RECT} = V_{RF} - |V_{th5}| \quad (5)$$

$$V_B = V_{RECT} - |V_{th7}| \quad (6)$$

$$V_B = V_{RF} - |V_{th5}| - |V_{th7}| \quad (7)$$

The voltage across the capacitor  $C_B$ ,  $V_B$  activates the transistor  $M_3$  to simultaneously charge the capacitor  $M_4$  with the transistor  $M_5$ . The voltage  $V_{GS}$  of transistor  $M_3$  is:

$$V_{GS,M3} = V_{RF} - V_B \quad (8)$$

$V_{GS}$  of  $M_3$  is equal to its threshold voltage the transistor  $M_3$  is deactivated when, so we can write:

$$V_{RF} - V_B = |V_{th3}| \quad (9)$$

Using (7) and (9), the output voltage can be calculated from (10).

$$V_{RECT} = V_{RF} - |V_{th3}| + |V_{th7}| \quad (10)$$

Therefore, if  $|V_{th7}| = |V_{th3}|$ , the capacitor  $C_L$  is charged on the value equal to the input voltage. The two PMOS,  $M_5$  and  $M_6$  diode transistors operate in a dynamic region have a ground (bulk) terminal that is not connected to the high voltage during a complete cycle. This problem causes the increase of the threshold voltage of the transistors connected to the diode and the bulk leakage current. The bulk bias circuit ( $M_8$ ,  $M_9$ ,  $M_{10}$ , and  $M_{11}$ ) is used to eliminate the body effect of transistors  $M_5$  and  $M_6$ . Since the effect of the threshold voltage of transistors  $M_3$  and  $M_4$  is neutralized by the bootstrap, the bulk bias circuit does not use for  $M_3$  and  $M_4$ , in order to have the maximum output voltage. Thus, the body of such transistors is connected to  $V_{RECT}$ . The power conversion efficiency of proposed rectifier is given by (11).

$$PCE[\%] = \frac{P_{OUT}}{P_{IN}} = \frac{V_{RECT}^2}{R_L \times P_{IN}} \times 100\% \quad (11)$$

With

$$P_{IN} = \frac{1}{T} \int_0^T V_{RF}(t) \times I_{RF}(t) dt \quad (12)$$

Where  $P_{OUT}$  and  $P_{IN}$  are the output power and input incident power respectively. Figure 5 presents the curve of power efficiency of the proposed full wave rectifier. At the input voltage 1.65V the power efficiency is about 74. 25%.

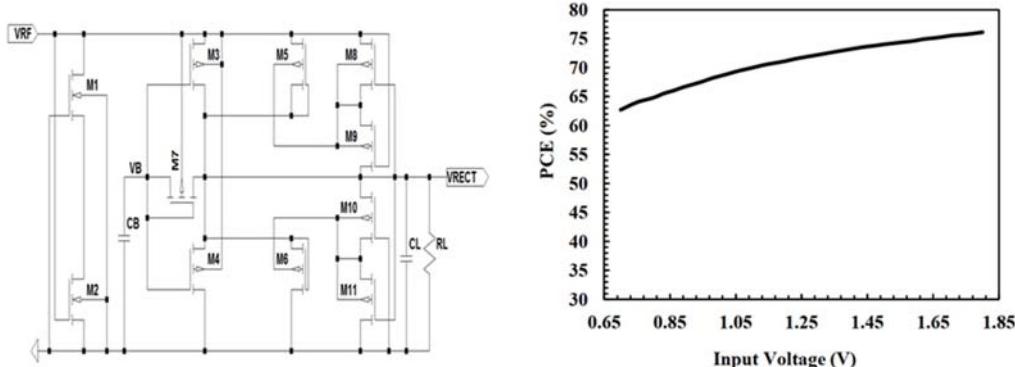


Figure 4. Proposed voltage rectifier

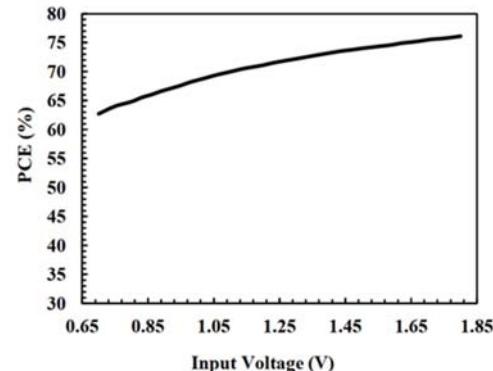


Figure 5. Curve of efficiency versus input voltage

### 2.3. Regulator

The regulator circuit comes after the full wave rectifier. The voltage regulator performs two main functions. The first is to regulate the output voltage to a preferred value and a preferred range for passive RFID UHF tag. The other is to protect the inner circuits from breaking at high RF input power. The basic topology of a voltage regulator is shown in Figure 8. It consists of an OTA, two regulation resistances and a voltage reference to generate a regulated voltage [10].

The output of a voltage regulator  $V_{reg}$  is given as follows. In an ideal case considering a finite open-loop gain  $A_{ol}$  the regulated voltage is given by:

$$V_{reg} = A_{ol}(V_p - V_m) \quad (13)$$

With

$$V_p = V_{ref} \quad (14)$$

we can write:

$$V_{reg} = V_{ref} \cdot \left( \frac{1}{\frac{1}{A_{ol}} + \frac{R_2}{R_2 + R_3}} \right) \quad (15)$$

If we consider an infinite open-loop gain for an ideal case so the simplifying calculates can we give:

$$V_{reg} \cong V_{ref} \cdot \left( 1 + \frac{R_3}{R_2} \right) \quad (16)$$

In (16) the output voltage of voltage regulator depends on the voltage reference  $V_{ref}$  and resistance  $R_2$  and  $R_3$ .

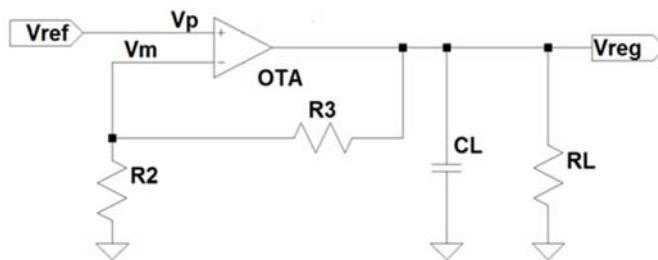


Figure 6. Voltage regulator schematic.

Figure 7 shows the proposed voltage regulator. It consists of four blocks, a diode NMOS regulator, a voltage reference an OTA and a voltage divider.

The NMOS diode regulator uses four series diode connected native NMOS transistor to limit large output of the voltage rectifier, which is on the order of dozens of tens of volts, to a relatively small swing.

One of characteristic of RFID passive tags is the fully integrated, RFID tag has not an external voltage reference, it means that the voltage reference used in voltage reference must be auto generated, even the power supply voltage. As shown in Figure 7, 1.6 V is generated directly by a reference self-biased voltage, instead of the conventional method for amplifying a low-precision reference voltage of the voltage pre-generated.

$M_{11}$  -  $M_{14}$  build a two cascade connection to increase the output resistance; all transistors operate in the low inversion region to reduce the power consumption. In the low-inversion region, the drain-source current is given by:

$$I_{sds} = I_{d0} \frac{W}{L} e^{q(V_{gs} - V_{th})(nkT)} \quad (17)$$

If the ratio  $W/L$  of the NMOS transistor  $M_{13}$  is made  $Q$  times larger than that of  $M_{14}$  and both have the same  $L$ ,  $V_{gs}$  of transistor  $M_{14}$  and  $M_{15}$  can be reformulated in terms current  $I_{sds}$  as

$$V_{gs13} = n \frac{kT}{q} \ln \left( \frac{I_{sds} L}{I_{d0} Q W} \right) + V_{th} \quad (18)$$

$$V_{gs14} = n \frac{kT}{q} \ln \left( \frac{I_{sds} L}{I_{d0} W} \right) + V_{th} \quad (19)$$

$$V_{gs14} = V_{gs13} + I_{sds} R_r \quad (20)$$

Using (17, 18 and 20) we can simply show that:

$$I_{sds} = \frac{nkt}{q} \ln Q \quad (21)$$

This current is independent of the *DC* power source and is much smaller, than the current operating in typical saturation region. With such a constant and small current, the voltage on the drain of transistor M<sub>12</sub> can be as stable and independent of the power supply. To minimize the lowest workable RF input power for the whole transponder, such a reference is expected to work under a power supply voltage as low as possible. The zero-threshold PMOS transistors M<sub>3</sub> - M<sub>4</sub> are used as the current mirror load to reduce the required V<sub>ds</sub> voltage drops. A low power regulator is simply a differential amplifier with feedback. The feedback detects the output voltage and compares it with the Vref provided by the voltage reference of the second step. For the differential amplifier, an NMOS amplifier is selected with an active PMOS load. In order to achieve low drop regulation and ensure that M<sub>18</sub> operates in the saturation region, the native MOS transistor with large W / L is used. Voltage divider used in proposed voltage regulator consists of resistances R<sub>4</sub> and R<sub>5</sub> can divide the output voltage value (vdd1) and give an output vdd2. Vdd2 is given by (22), with vdd2=1V to obtain vdd1=0.5V R<sub>5</sub> must be equals R<sub>4</sub>.

$$V_{dd1} = \frac{R_5}{R_5 + R_4} \times V_{dd2} \quad (22)$$

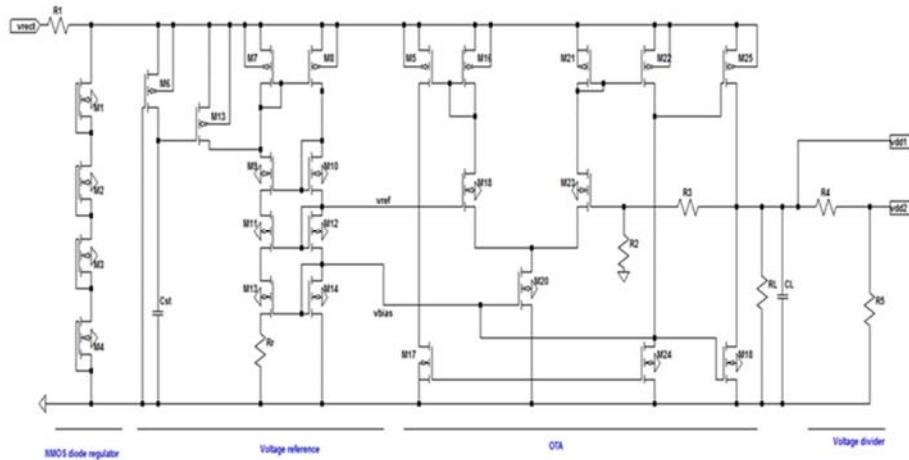


Figure 7. Proposed low power voltage regulator.

### 3. RESULTS AND ANALYSIS

The simulation results of proposed power generating circuit are introduced in this section. Figure 8 shows the transient response of vdd1 and vdd2. Vdd1 and vdd2 with different input power levels which changes from -22dBm to 14 dBm are shown in Figures 9 and 10 respectively. In -22dBm input power, the obtainable largest conversion efficiency is still 29.15%, which is higher than the reported results shown in comparison table. With 29.15% power conversion efficiency the communication distance of RFID system is about 10m. Table 1 introduces our work efficiency compared to other works [5], [11], [12], [13]. The layout for the power generating circuit for an UHF RFID tag circuit is shown in Figure 11. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double layer guard rings. The layout is done by respecting following items; design rules (DRM, MRC and Density) and designer constraints information (constraint manager, text). It occupies an active area of 0.25mm<sup>2</sup>.

Table 1. Comparaison table

Ref.	Efficiency	Minimum input power	Range	Carrier frequency	CMOS Process
This work	28.49 %	4.7μW **, 15.85 μW **	52 λ	900 MHz	180 nm
[5]	26.96 %	5.01μW **, 15.08μW **	45 λ	900 MHz	90 nm
[10]	14.5 %	63μW *	28.2 λ	900 MHz	0.5 um
[11]	10.94 %	-	21.3 λ***	450 MHz	0.25 um
[12]	-	12.6 μW	5.6 λ***	2.4 GHz	1 um

\*normalized for 3V generation, \*\* normalized for 1V generation, \*\*\* normalized for 4 W EIRP source.

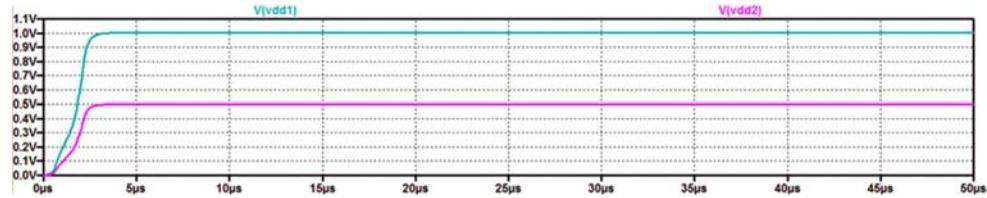


Figure 8. Transient response of proposed generating circuit.

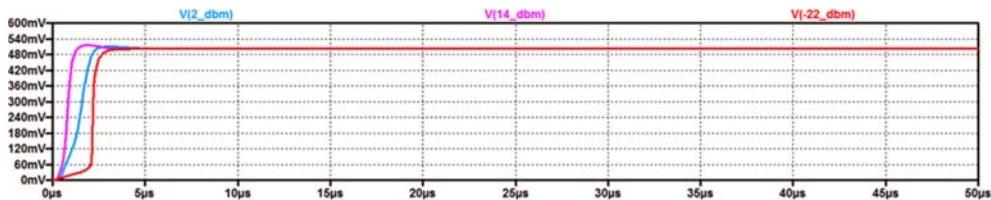


Figure 9. Transient response of vdd1 with different input power levels.

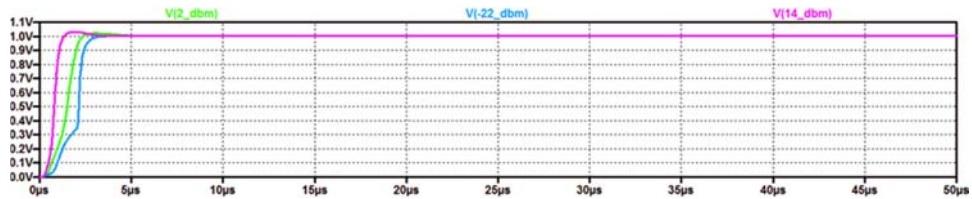


Figure 10. Transient response of vdd2 with different input power levels.

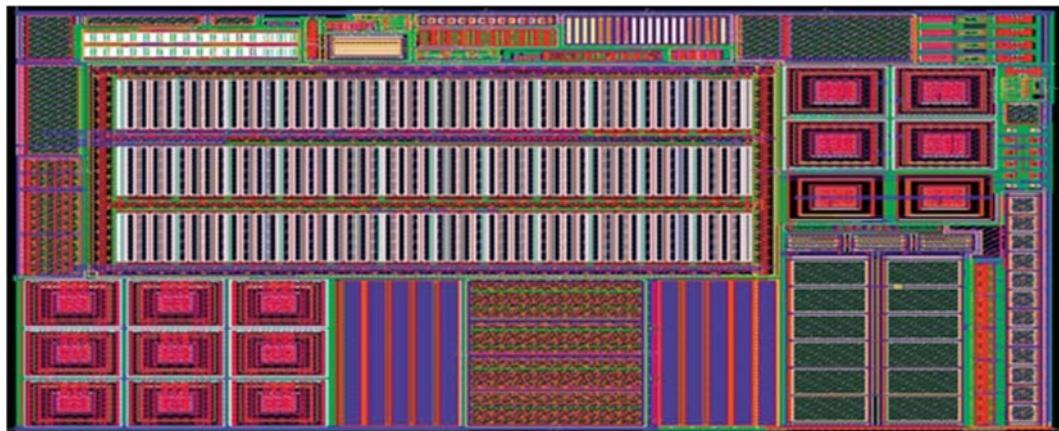


Figure 11. Layout of proposed power generating circuit.

#### 4. CONCLUSION

In conclusion, a new power generating circuit for a UHF RFID transponder with multiple output supply voltage has been successfully designed in TSMC 180 nm technology. Circuit design, simulation, analysis and layout design are all included in this study. The performance of the proposed power generating circuit is enhanced a good accuracy of the voltage supply which is stable and independent of the power voltage levels as the power supply for a UHF passive RFID tag.

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